G-COE PICE International Symposium and IEEE EDS Minicolloquim on
Advanced Hybrid Nano Devices: Prospects by World's Leading Scinetists
Tokyo Tech., October 4 and 5, 2011

Challenges of Heterogeneous Integration on CMOS

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Information
Communication
Energy
Semiconductor Solution Research

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Pursuing Excellence

Outline

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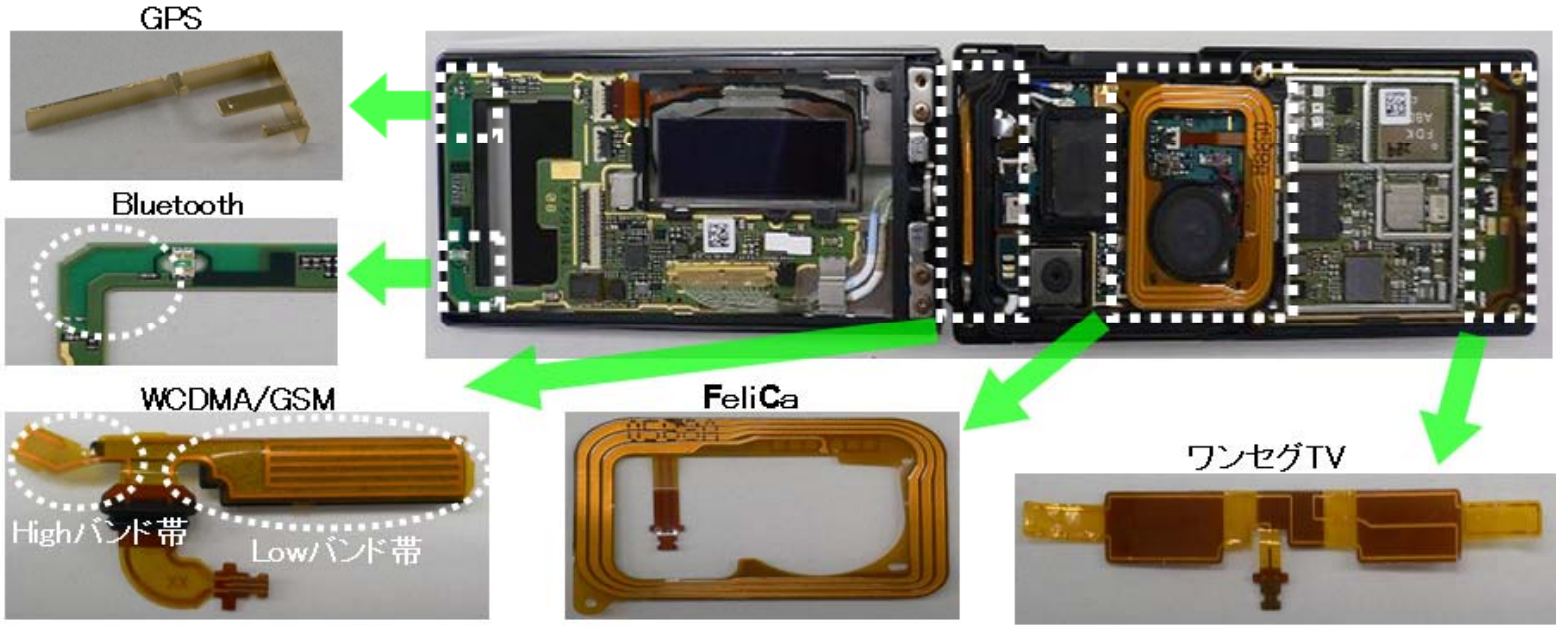
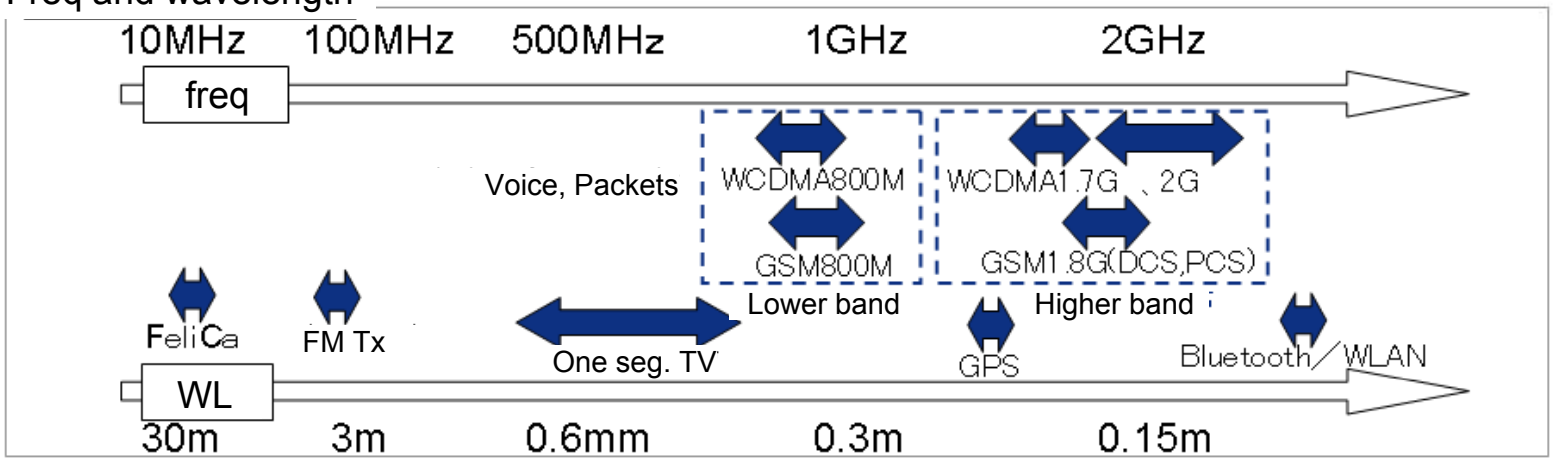
1. Introduction Why RF CMOS?
2. Our RF CMOS development
   - Why do we expect heterogeneous integration on CMOS ?
3. Our approach to heterogeneous integration: Novel wafer shuttle technique.
4. Summary

Recent mobile phone



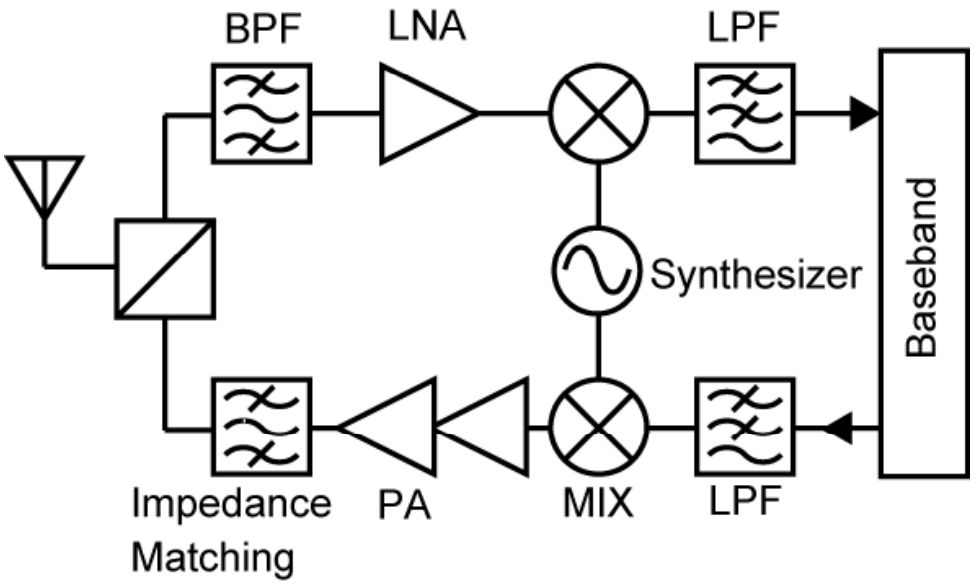
Freq and wavelength



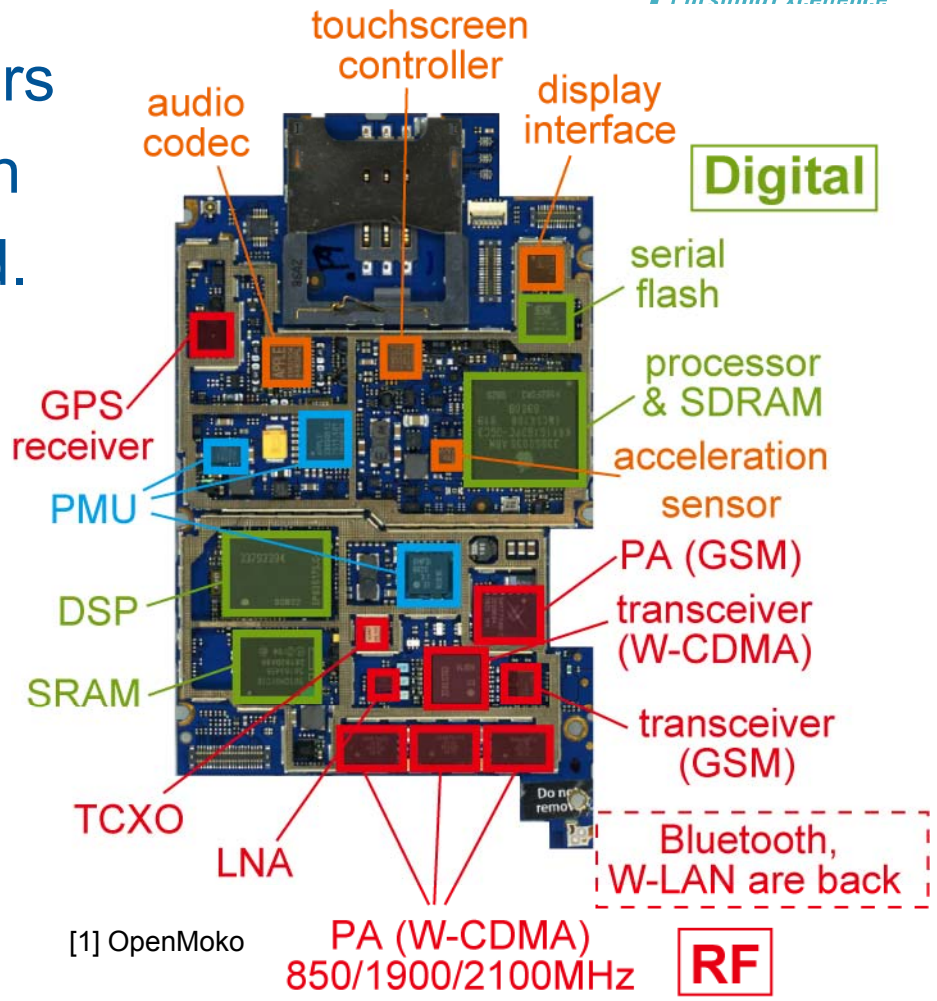
Courtesy of Hideyuki Saso, Vice President, Fujitsu

Mobile phone

Wideband RF frontend that covers multiple wireless applications with only one chip is in highly required.



L and C limit operational frequency



[1] OpenMoko

PA : Power Amplifier
MIX : Mixer
LPF : Low Pass Filter
LNA : Low Noise Amplifier

Mutiband/multimode transceiver

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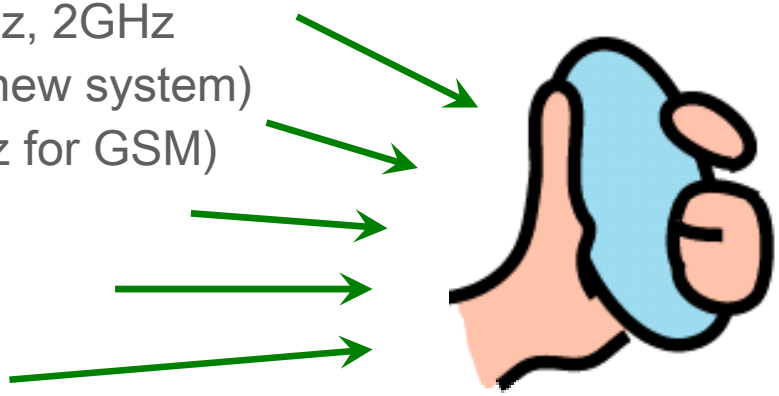
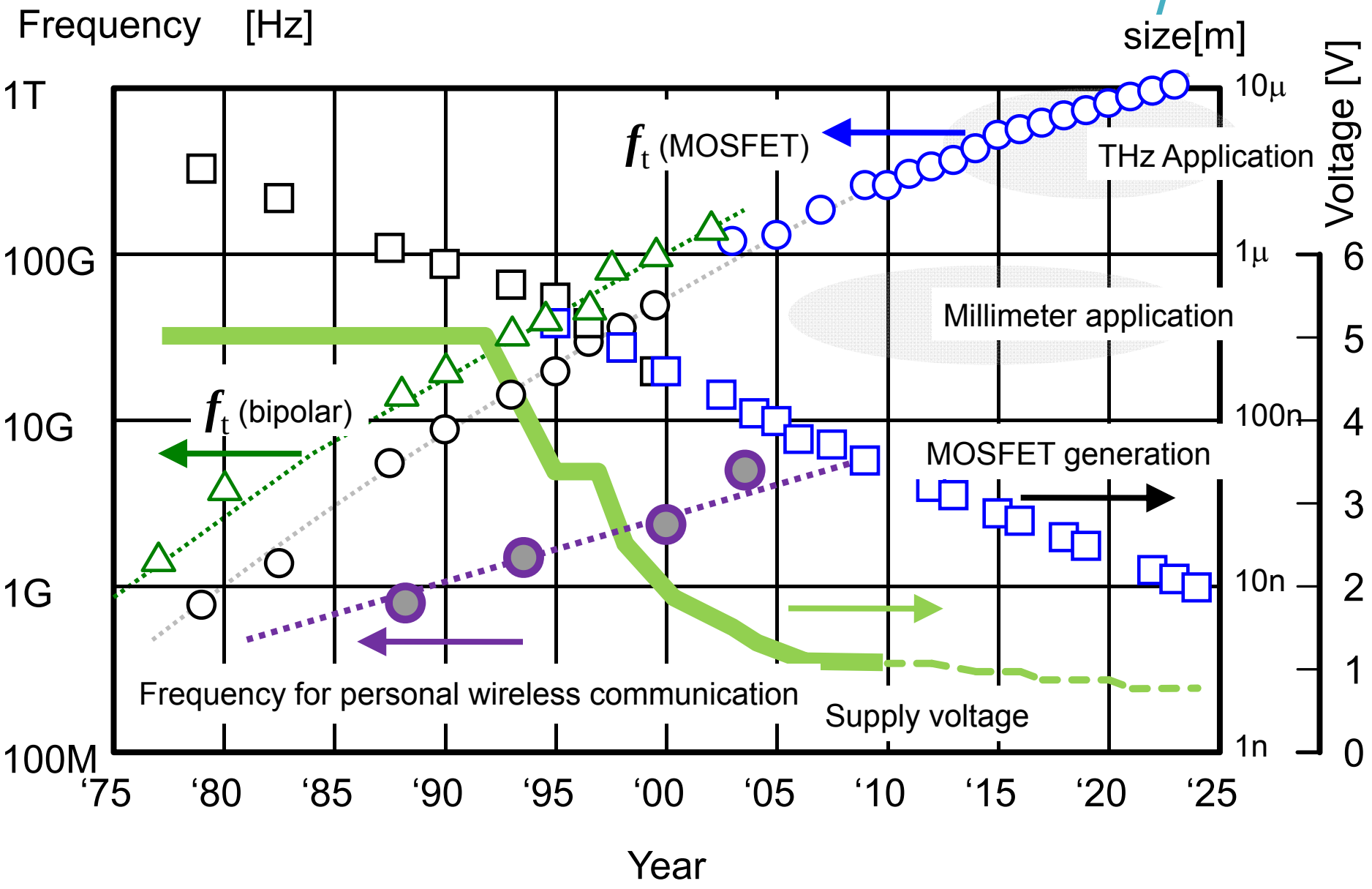
- Many wireless standards (400MHz – 6GHz)
  - Mobile phone 800MHz, 1.5GHz, 1.9GHz, 2GHz
    (+700MHz, 900MHz, 1.7GHz for the new system)
    (+800MHz, 900MHz, 1.8GHz, 1.9GHz for GSM)
  - WLAN 802.11b/g, Bluetooth 2.4GHz
  - WLAN 802.11a/n 4.9GHz – 5.875GHz
  - GPS 1.2GHz/1.5GHz
  - DTV 440MHz – 770MHz



One terminal

- User's viewpoint
  - User wants to connect network whenever, wherever, whomever, and whatever.
- System viewpoint
  - Improvement of frequency usage efficiency
- Multiband/multimode wireless communication is indispensable.

Miniaturization of MOSFET/CMOS



Miniaturization and Diversification

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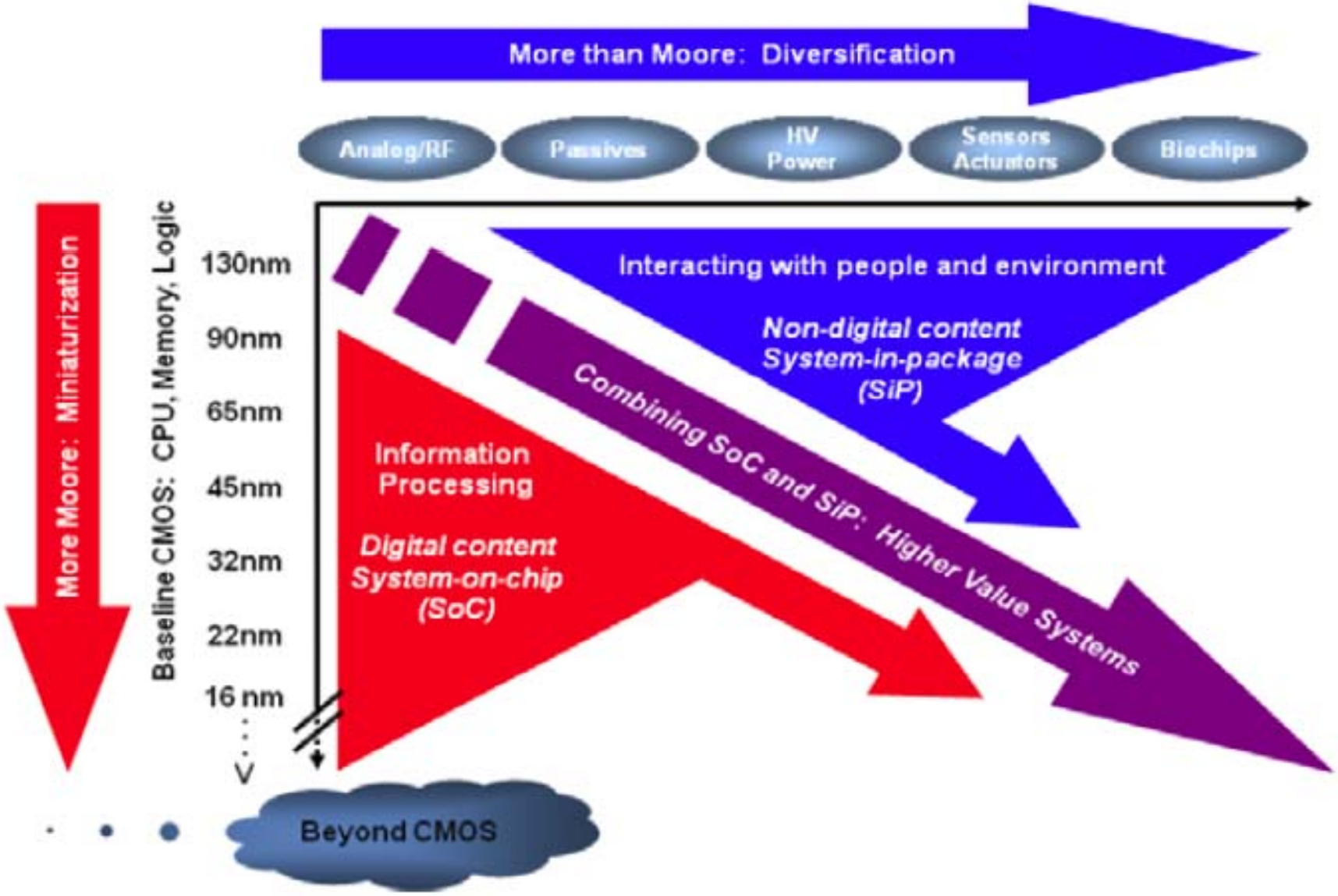

Digital vs. Analog/RC LSI

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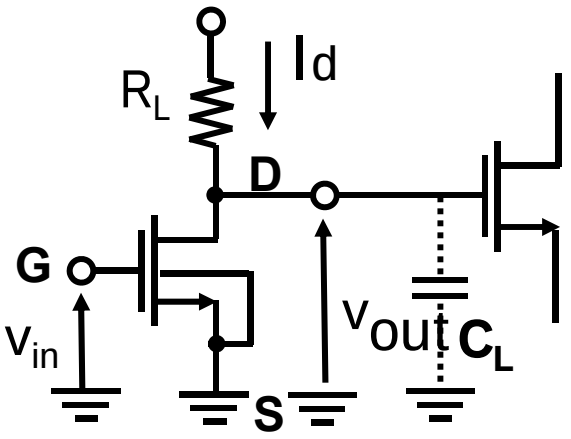
- What is difference?

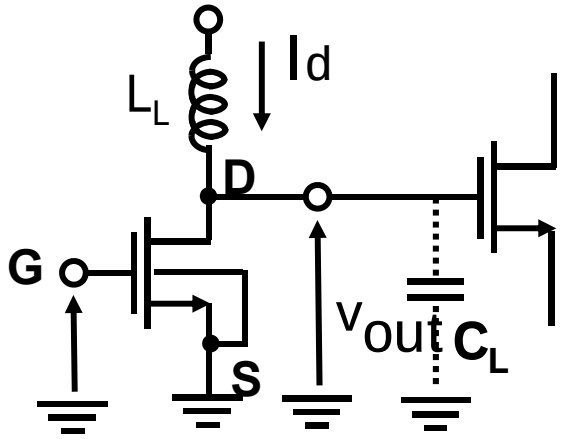
Scaling

- CMOS device miniaturization has brought
  - High-speed/high-frequency,
  - Low consumption power, and
  - Chip area reduction.
- **Chip area reduction is directly related to lowering cost.**
- If there is not area reduction (= cost reduction), miniaturization is meaningless.
- Area reduction of circuit using miniaturized devices is essential!

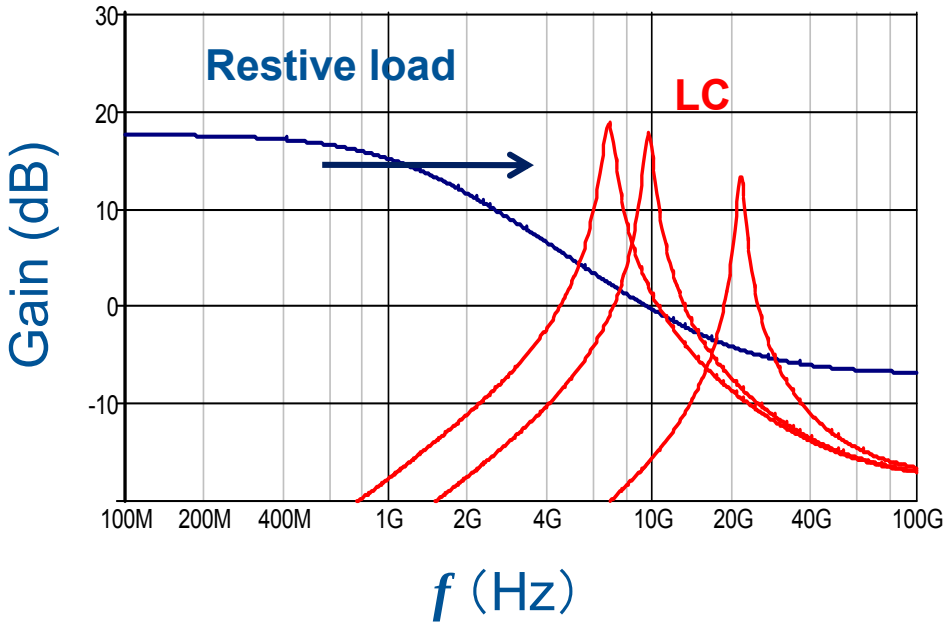
RF CMOS



Restive load



Typical LNA using LC resonance



- Gain of R-load LNA is degraded at high freq because of RC component.
- LNA has sufficient gain at high freq using LC resonance.

Digital vs. RF CMOS circuit

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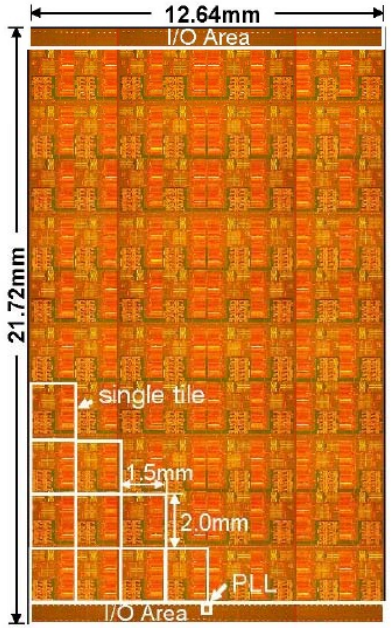
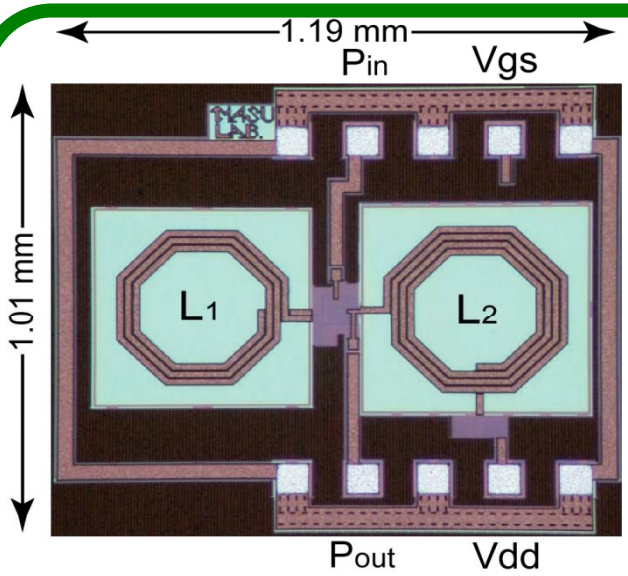
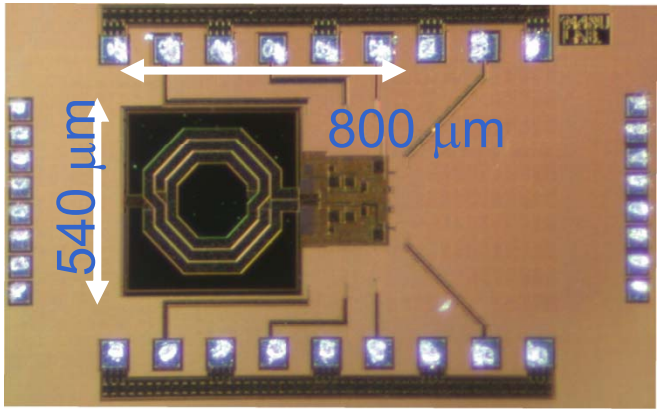


Many Core10^8Tr/3mm^2



LNA（Low Noise Amp）

RF CMOS



VCO（Voltage Controlled Oscillator

- Area reduction is essential in CMOS scaling. Passive devices such as inductor, resistor (including wire) and capacitors consume large area. CMOS devices are miniaturized, however the passives are not miniaturized!
- Challenge of analog/RF circuit design is to reduce the area penalty of passives; ideally elimination of passives.

Challenges in RF CMOS

- RF CMOS has sufficiently high f_t and f_{max}
  - No need of scaled MOS. 0.18μm/0.13μm CMOS is enough for GHz application.
  - Requirement of monolithic integration digital modulation/demodulation and analog/RF signal processing. Passives such as inductor prevent the chip area from reduction.

Challenges in RF CMOS

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Two approaches

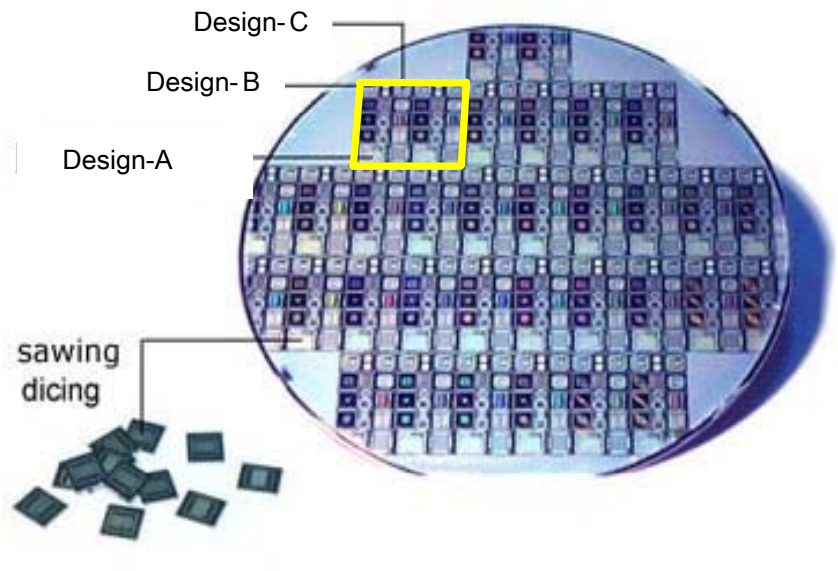
- Heterogeneous integ
- Integ with diverse functionalities
- More than Moore

- RF using mature (0.35, 0.18μm) CMOS
- Performance enhancement with other technologies such as MEMS.
- Integ with digital by SiP, 3D, etc.

- Miniaturization
- Scaling
- More Moore

- RF/Analog/Digital one chip (SoC)
- Area reduction of RF is indispensable.

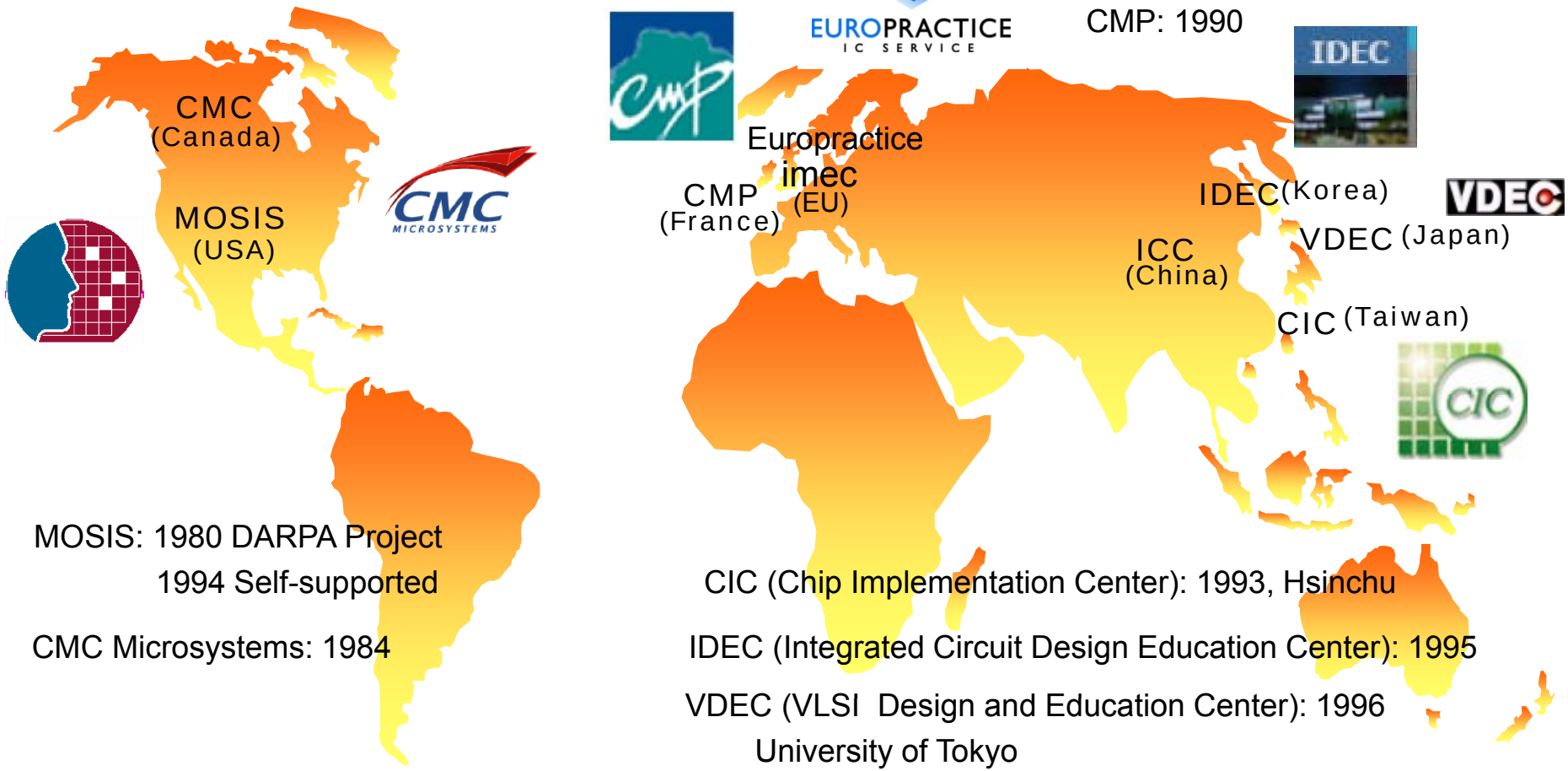
Our research style using shuttle service



Shuttle service

- Designers design CMOS circuit using PDK (Process Design Kit) supplied from foundry.
- Foundry fabricates CMOS circuit. Designer receive CMOS chip.
- Designers evaluates CMOS circuits.

Worldwide Service Institutes



MOSIS: 1980 DARPA Project
1994 Self-supported

CMC Microsystems: 1984

Europractice: 1989

CMP: 1990

CIC (Chip Implementation Center): 1993, Hsinchu

IDEC (Integrated Circuit Design Education Center): 1995

VDEC (VLSI Design and Education Center): 1996
University of Tokyo

ICC (IC Technology and Industry): 2000, Shanghai

Major IC Design and Chip Implementation Service Institutes

Worldwide Service Organizations

TOKYO TECH

Country	USA	Canada	France	Japan	China	Korea	Taiwan
Institutes	MOSIS	CMC	CMP	VDEC	ICC	IDEC	CIC
Established	1980 1994	1984	1990	1996	2000	1995	1993
EDA Tool Vendors	X	NA	7	9	5	16	17
Fabricated Chips (#)	NA	380	391	254	120+176	250	1621
Processes Provided (#)	26	6	15	8	15	8	14
Advanced Process	40nm	65nm	40nm	40nm	90nm	40nm	40nm
Packaging	○	○	◎	○	○	○	◎
Testing	X	○	X	○	○	○	◎
Training Coursed	X	NA	X	○	NA	◎	◎

Remark：○ ：Fair Service; ◎ ：Excellent Service ；X ：No Service。

Source: 2009 CMP Annual Report

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Challenges in RF CMOS

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Two approaches

- Heterogeneous integ
- Integ with diverse functionalities
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- RF using mature (0.35, 0.18μm) CMOS
- Performance enhancement with other technologies such as MEMS.
- Integ with digital by SiP, 3D, etc.

- Miniaturization
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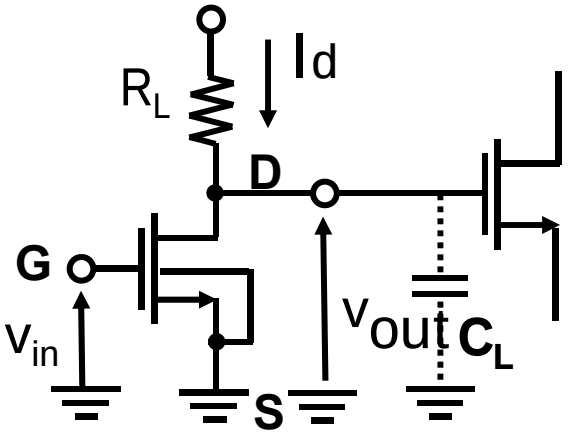
- RF/Analog/Digital one chip (SoC)
- Area reduction of RF is indispensable.

RF CMOS



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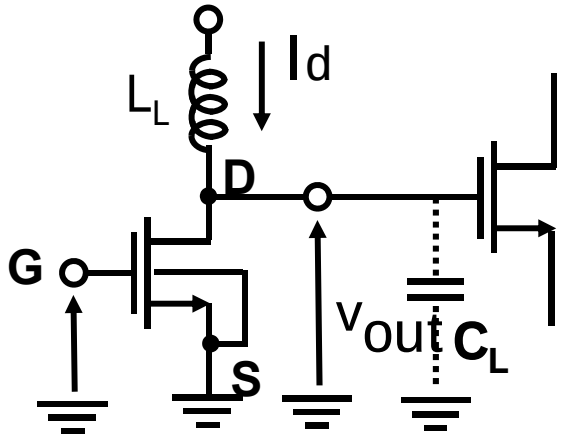
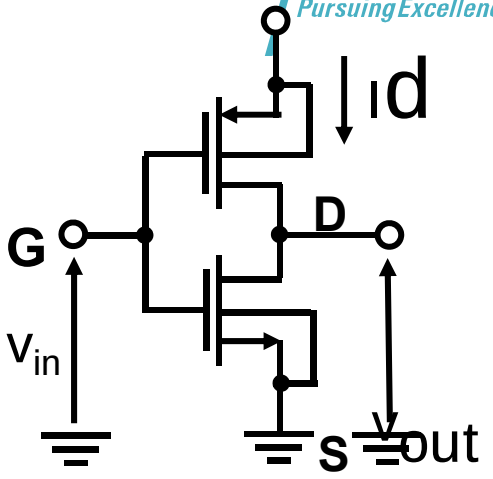
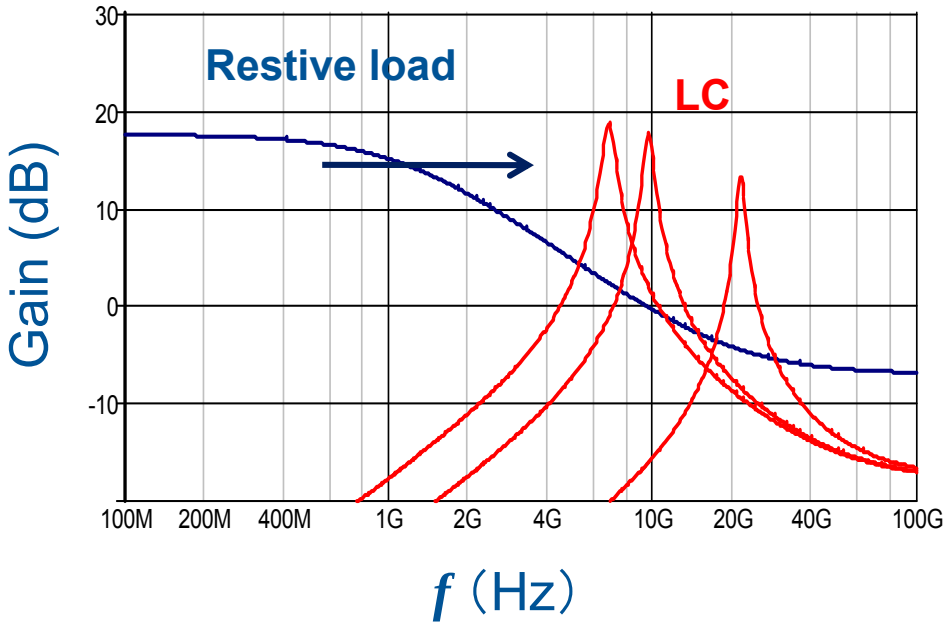


Typical LNA using LC resonance





- Gain of R-load LNA is degraded at high freq because of RC component.
- LNA has sufficient gain at high freq using LC resonance.
- Our approach: CMOS-inverter base circuit components.

Breakthroughs

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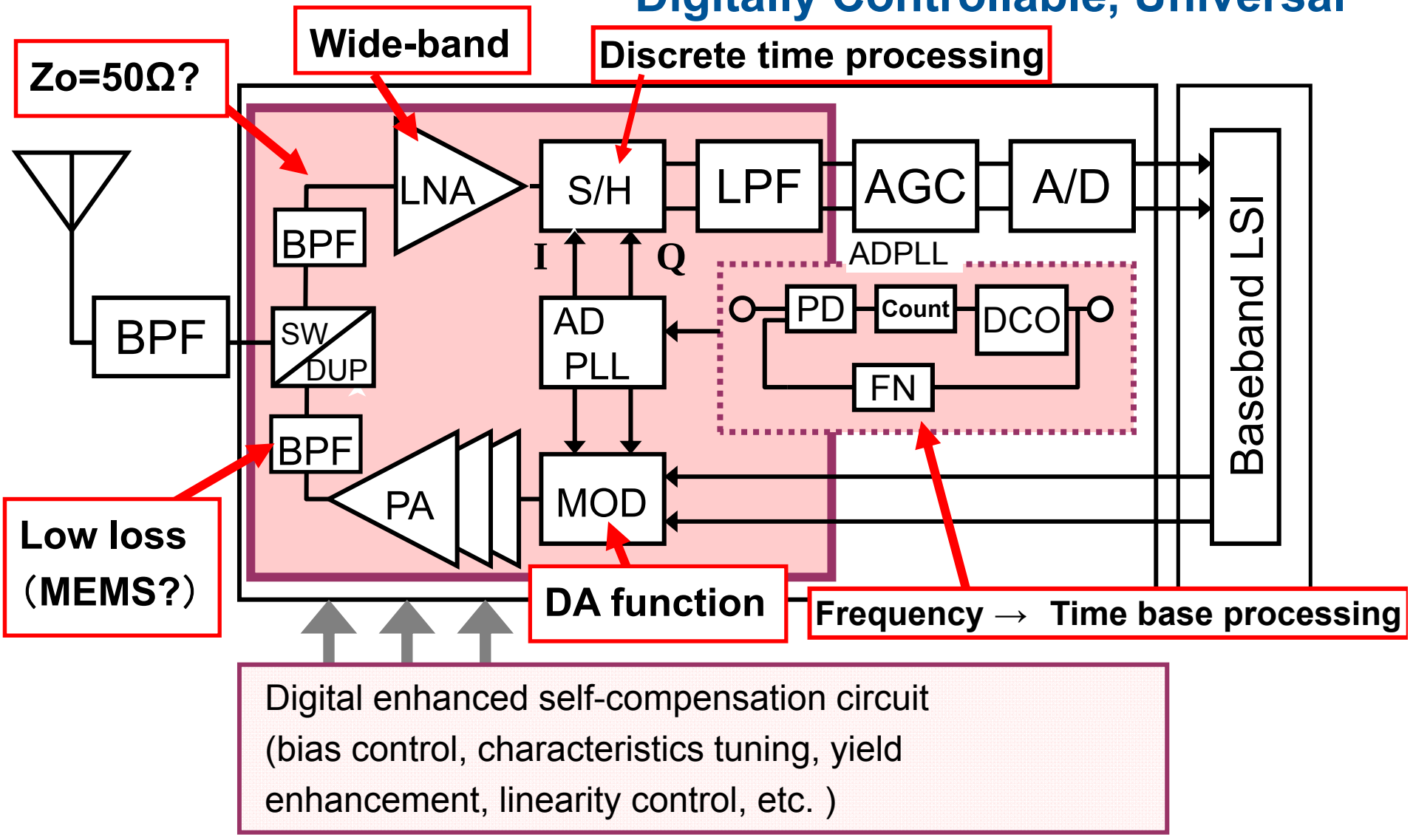
Scalable, Multi-band, Wide-band, Digitally Controllable, Universal



Our recent work of scalable RF CMOS in 2008-2010

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●	Scalability	●Discussion of scalability of the conventional topology
①	LNA	●Wideband using Cherry-Hooper & active feed-back
②	LNA+VGA	●High-gain LNA+VGA by multi-stage inverter ●Gain control using MOS-SW
③	Ring-VCO	●Low phase technique using Injection-lock and latched inverter
④	PLL using ring-VCO	●Freq synthesizer using PLL combination
⑤	PA	●Stacked CMOS for high-power output
⑥	RF modulation block	●RF signal generation using time-to-analog conversion ●QPSK signal generation using phase selection and injection lock techniques
⑦	RF demodulation block	●Passive mixer (on going)
⑧	Power supply	●On-chip LDO

Inverter base LNA

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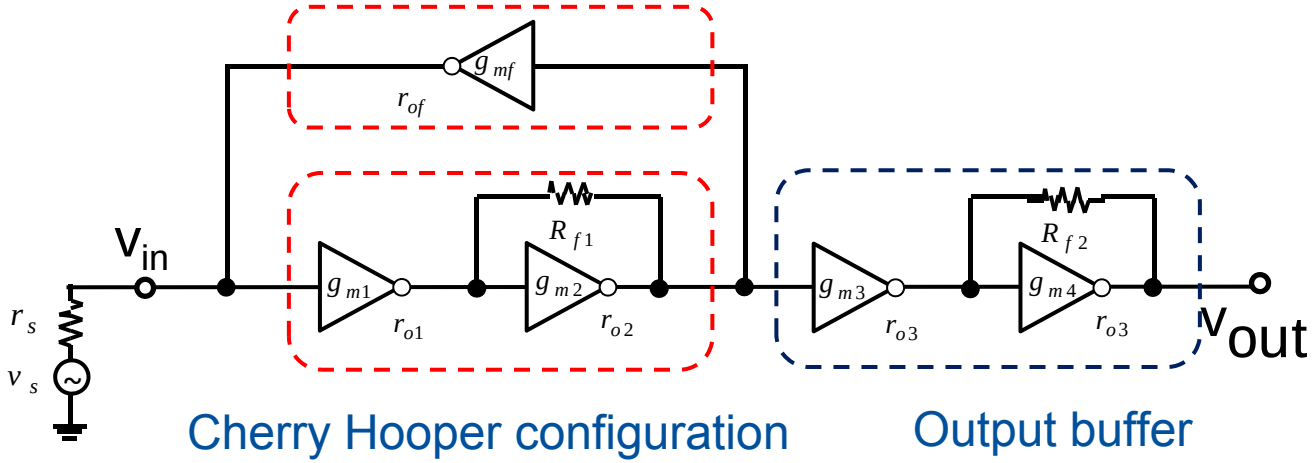
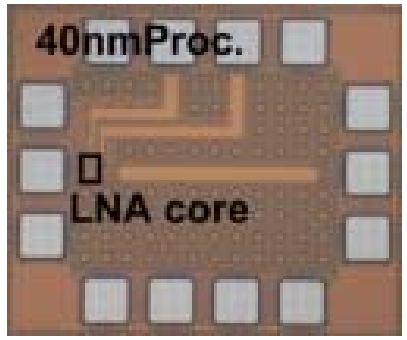
Active feedback for wideband



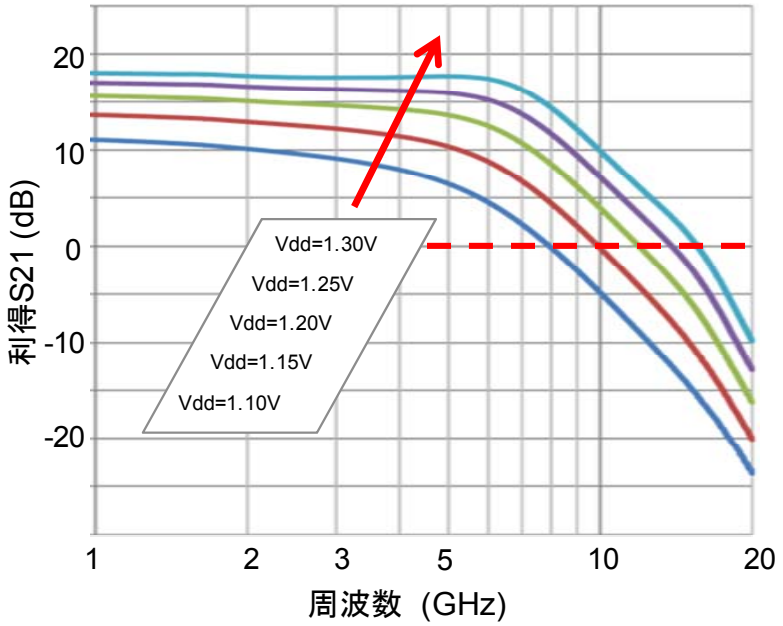
Cherry Hooper configuration

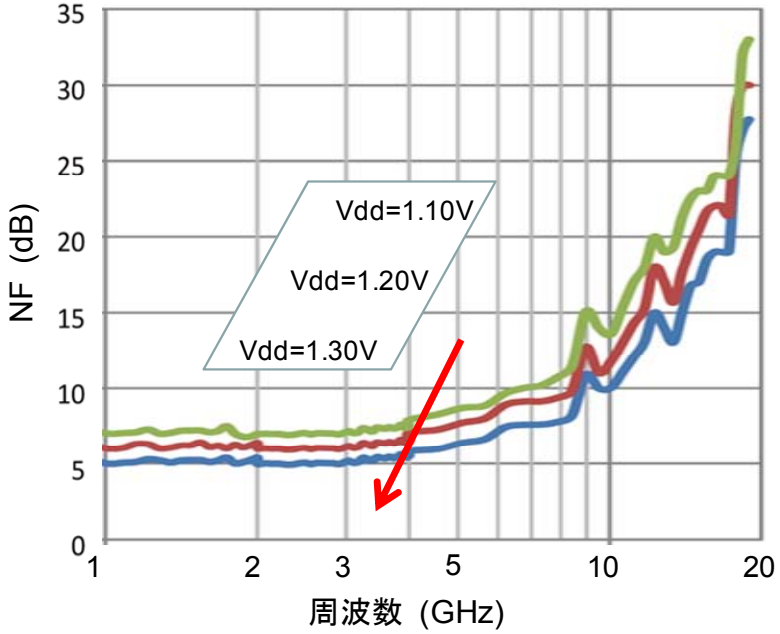
Output buffer



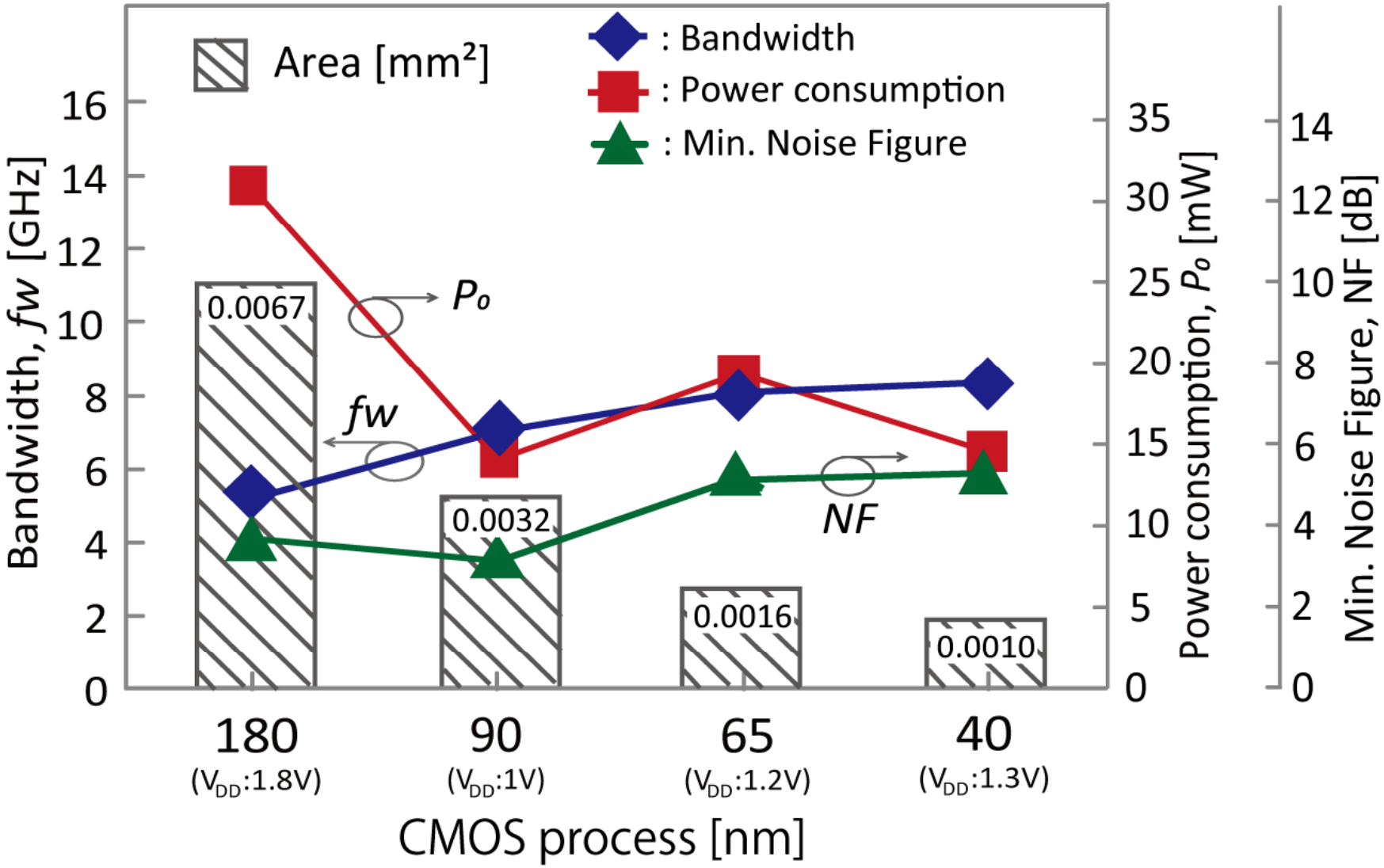
Supply voltage: 1.1 V

Area: 40 x 26 μm²





Performance of Scalable RF CMOS LNA



Injection locked differential VCO

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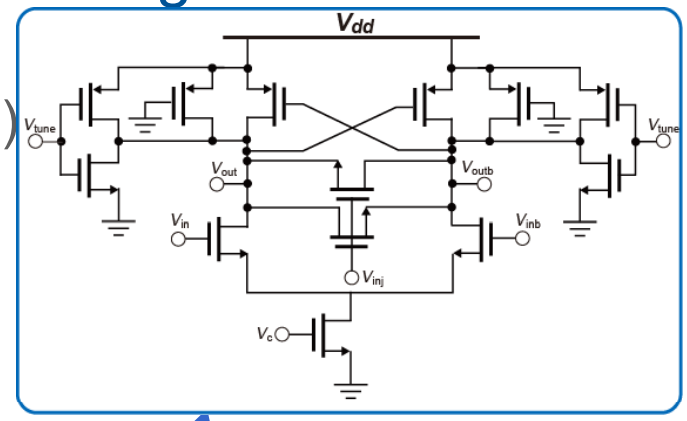
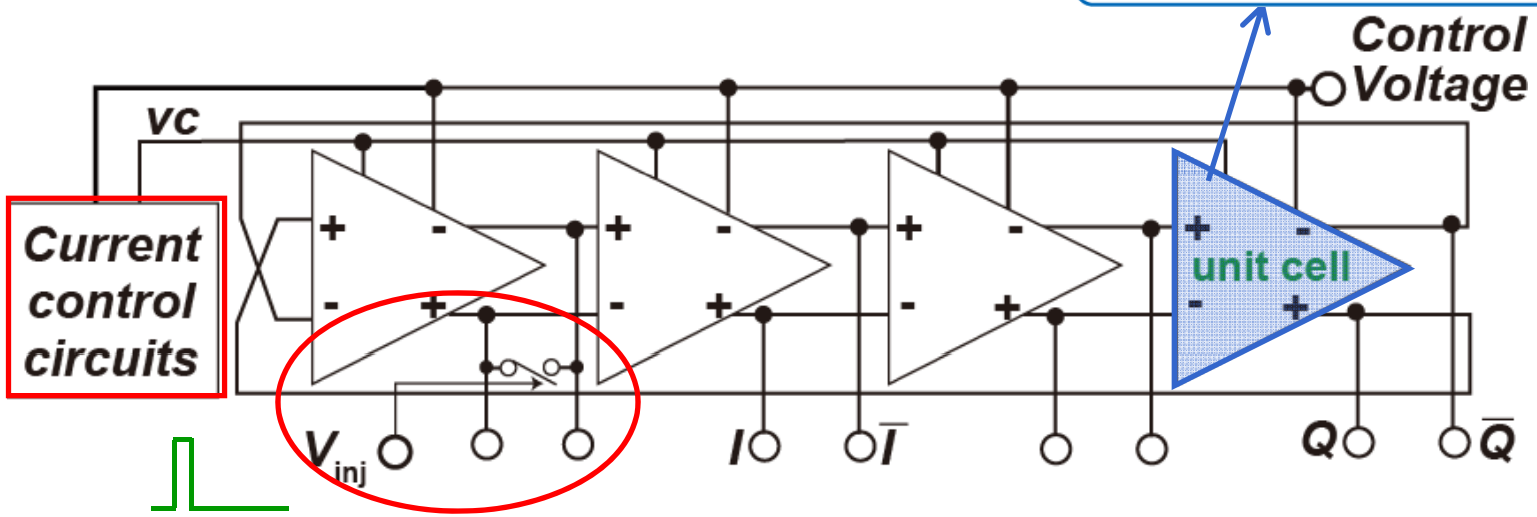
Features (180nm CMOS process)

- 4-satage Ring-VCO
  - I/Q signal generation (0°, 90°, 180°, 270°)
- Half Integral subharmonic Injection locking
  - High freq resolution (40MHz)
  - Low-phase noise (comparable to LC-VCO)
  - (–120dBc/Hz@1MHz offset)
- Current control
  - Wideband operation (1-2GHz)





Injection lock performance of D-VCO

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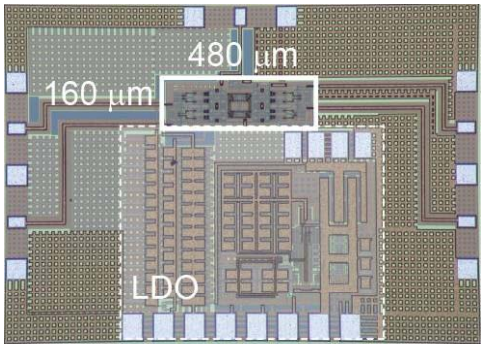
Chip photo



Ring-VCO performance

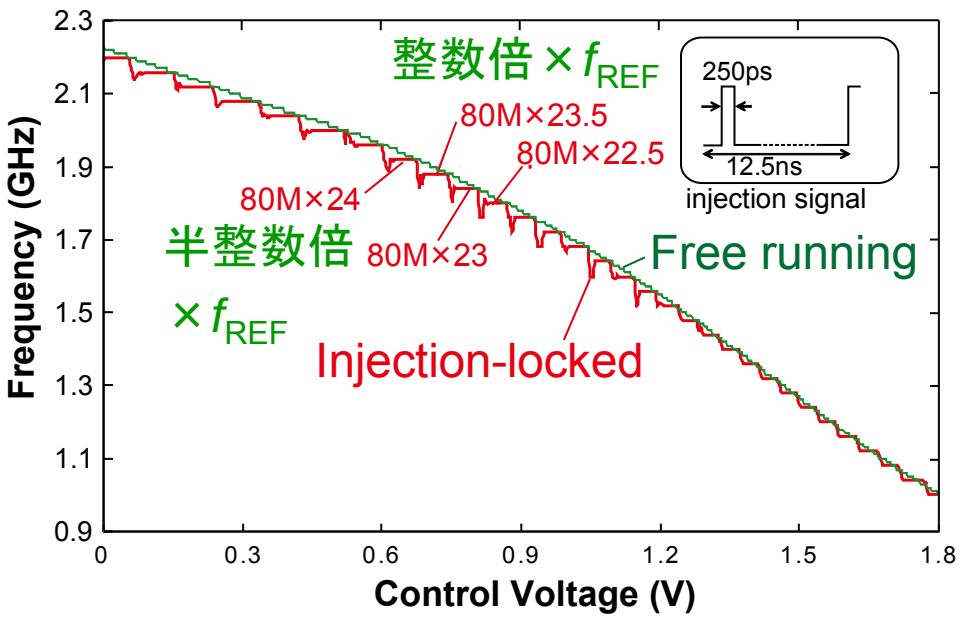
Osc freq (free running):1.0G – 2.2G

Power: less than 62mW

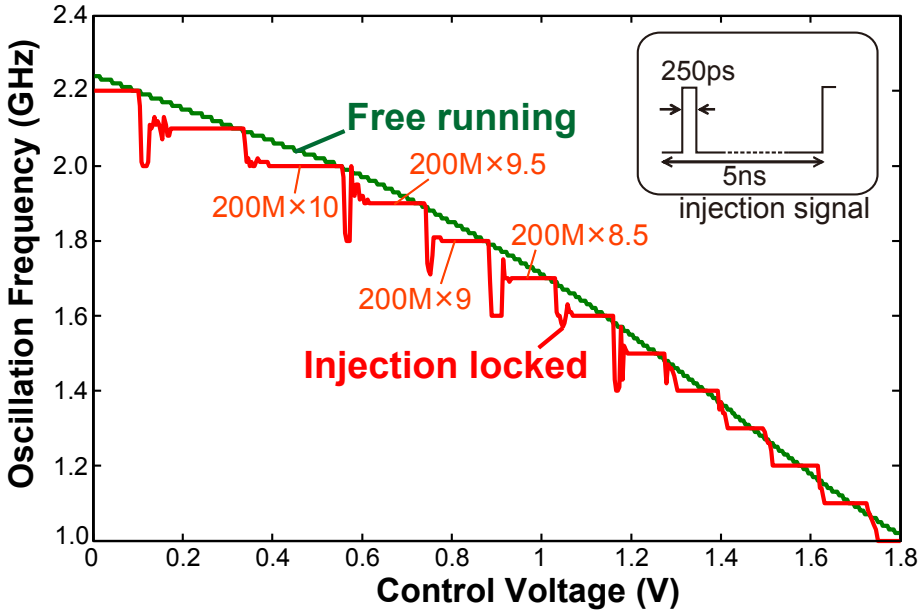
Phase noise@1MHz offset

:–102dBc/Hz @1.44GHz

Freq performance (ref:80MHz)



Ref: 200MHz



Phase noise of injection locked D-VCO

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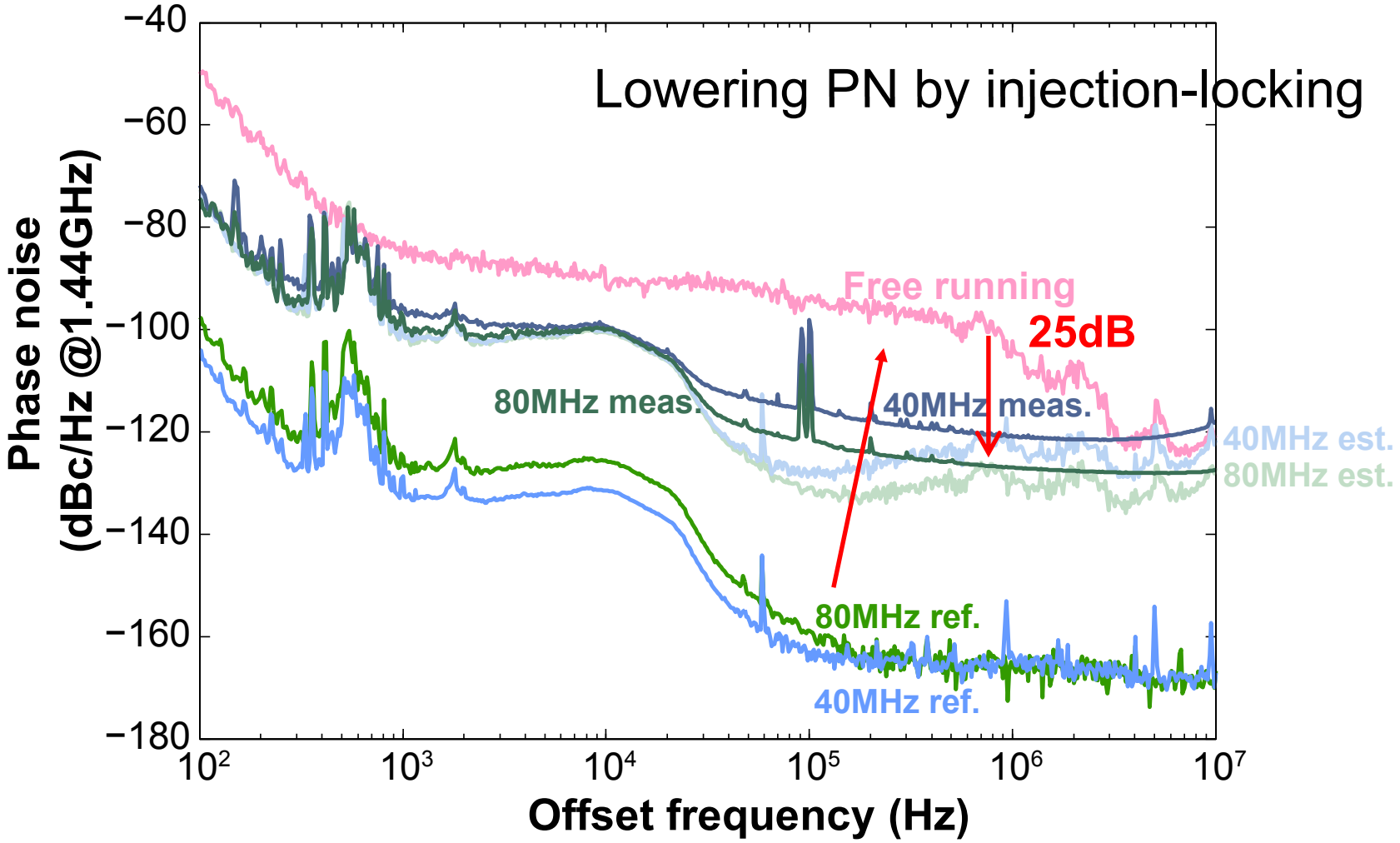
PN@1MHz offset@1.44GHz

-121dBc/Hz (input pulse width:250ps 40MHz): 20MHz resolution

-127dBc/Hz (input pulse width: 250ps 80MHz): 40MHz resolution



PLL using ring-VCO

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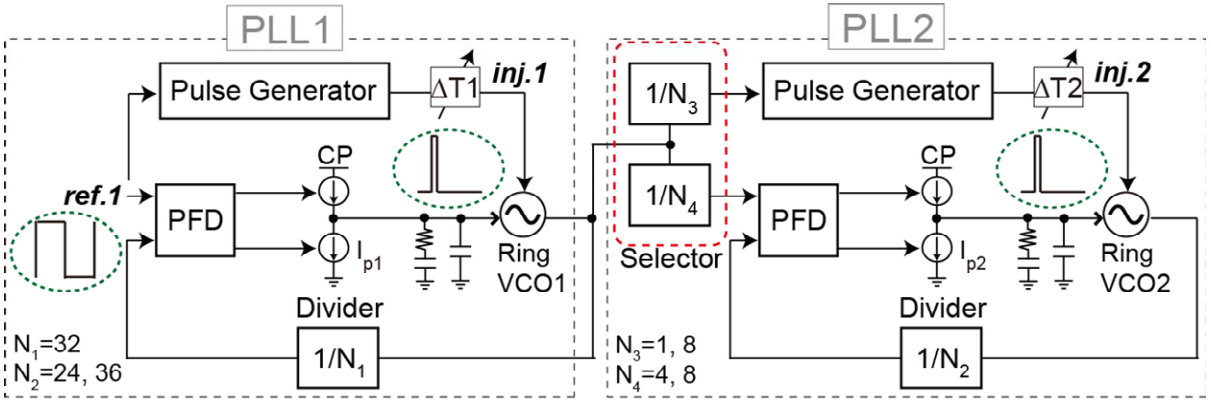
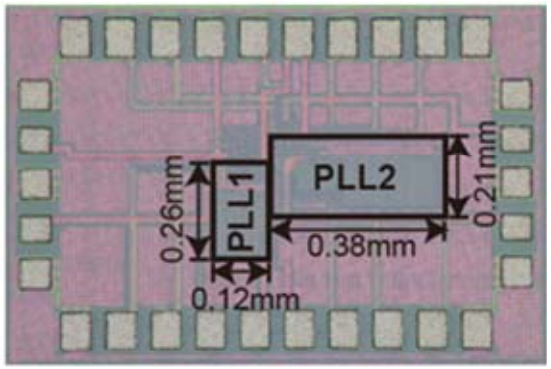
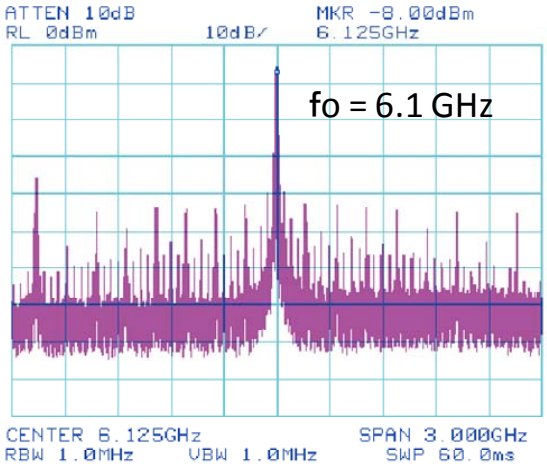
PLL using injection-locked ring-VCO



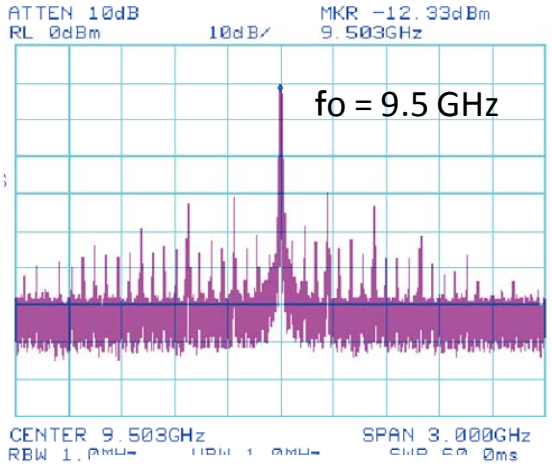
(a) 2ステージPLL回路の構成



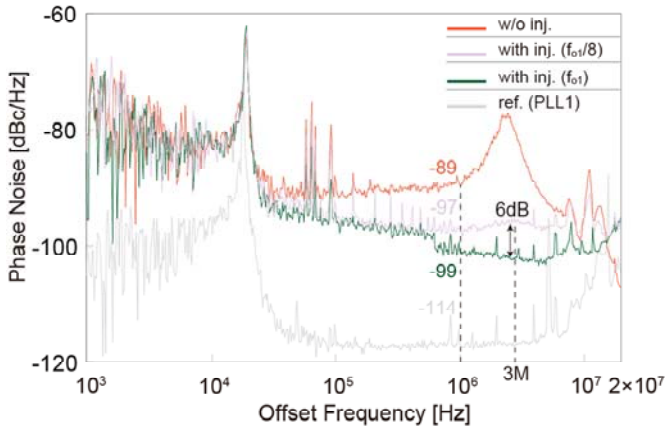
(b) 90nmCMOSによる試作チップ



(c) 6.1 GHz 発振時



(d) 9.5 GHz 発振時



(e) 位相雑音特性（6.1 GHz）

Challenges in RF CMOS

Two approaches

- Heterogeneous integ
- Integ with diverse functionalities
- More than Moore

- RF using mature (0.35, 0.18μm) CMOS
- Performance enhancement with other technologies such as MEMS.
- Integ with digital by SiP, 3D, etc.

- Miniaturization
- Scaling
- More Moore

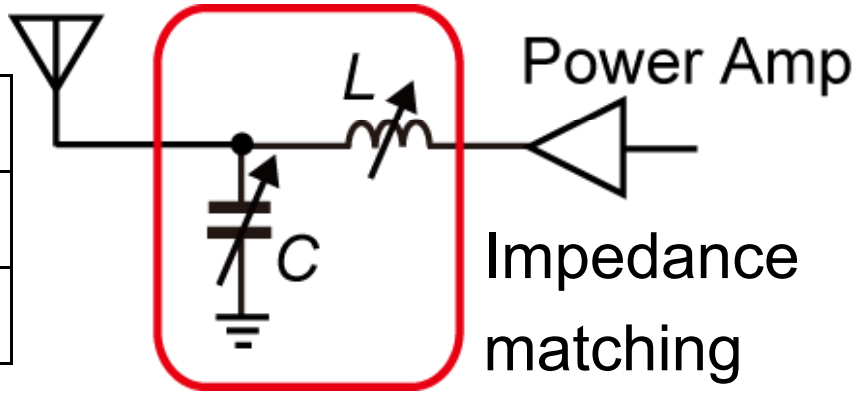
- RF/Analog/Digital one chip (SoC)
- Area reduction of RF is indispensable.

Purpose

Z_{out} = 5Ω of PA matching with 50Ω of antenna

required L and C tuning range at 0.8~6GHz

freq (GHz)	L (nH)	C (pF)
0.8	3.0	12.0
6.0	0.4	1.6

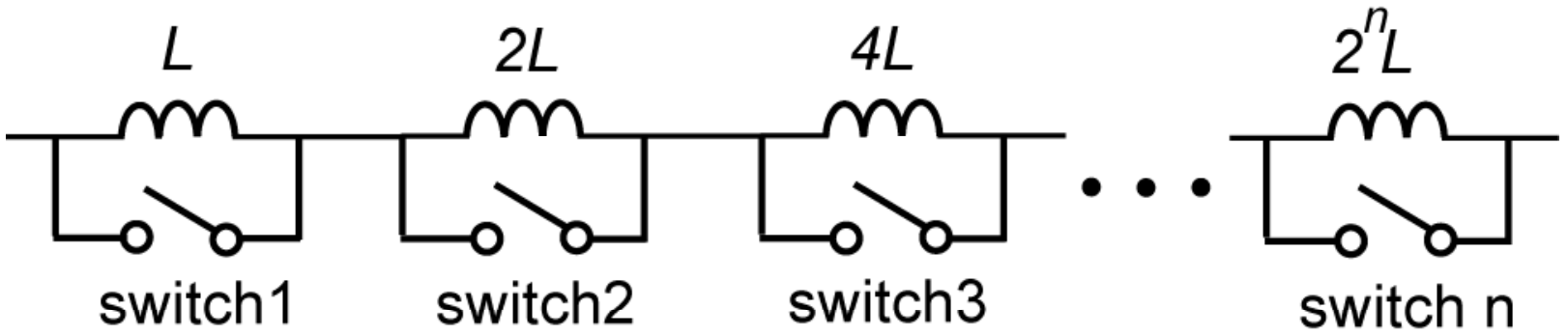


Purpose: Variable inductor for wideband RF-frontend

Variable inductor requirements

- Wide inductance tunable range for wideband operation
- High Q factor to reduce loss
- High self resonant frequency for higher available frequency

N-bit control variable inductor



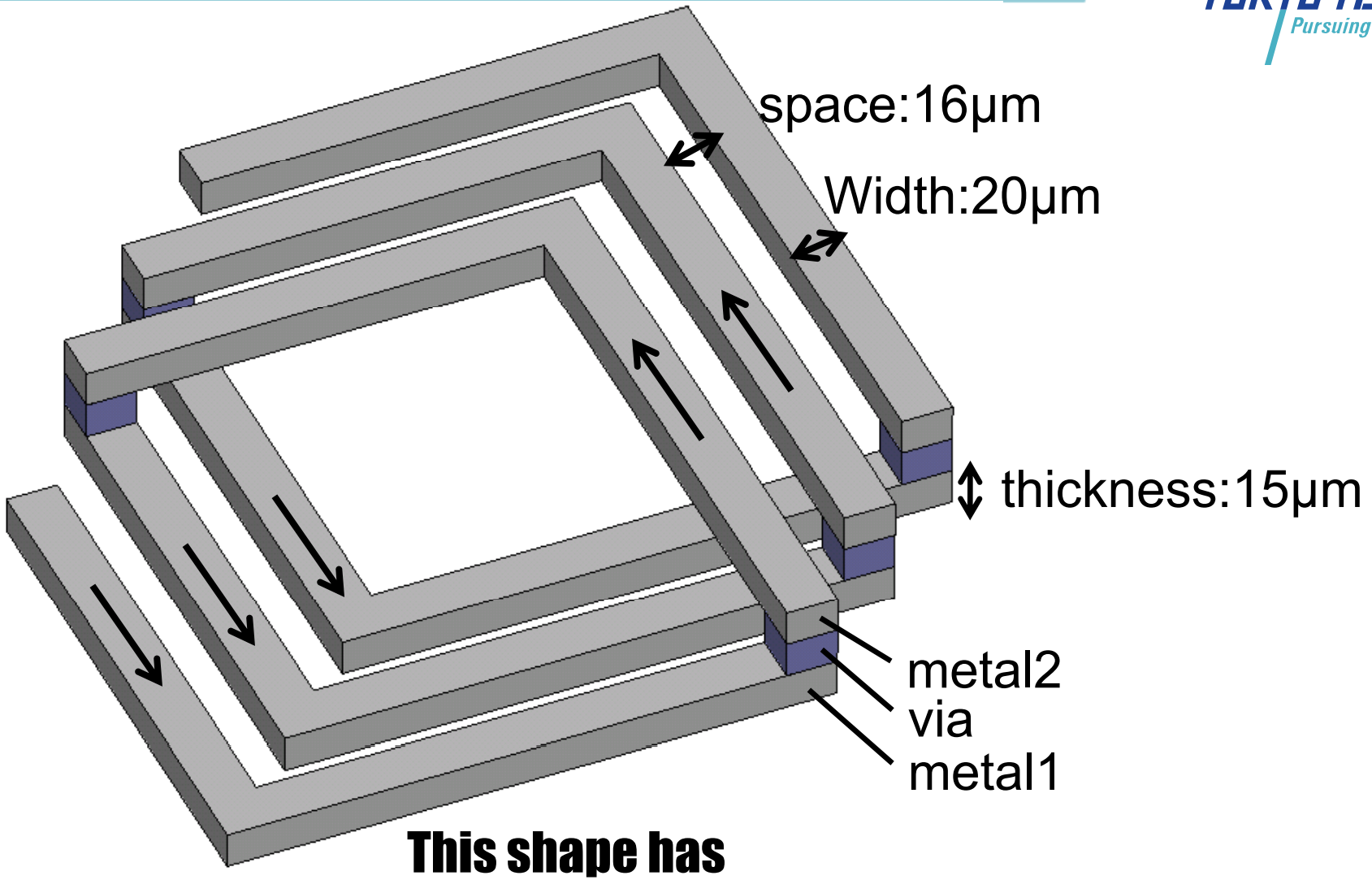
- Controlling inductance with N switches
- Decreasing inductance by switching on
- Switch type variable inductor can easily improve tunability
- High resolution with fewer switches eg) 8 value with 3 switches

CMOS process can realize this but loss is large

Switches and inductors with lower loss can be achieved by using MEMS

Thick metal and movable structure

Planar solenoidal inductor



This shape has

- Capability of attaching switch depending on number of turn
- Large $L_{+mutual}$ and small $L_{-mutual}$ to improve Q-factor

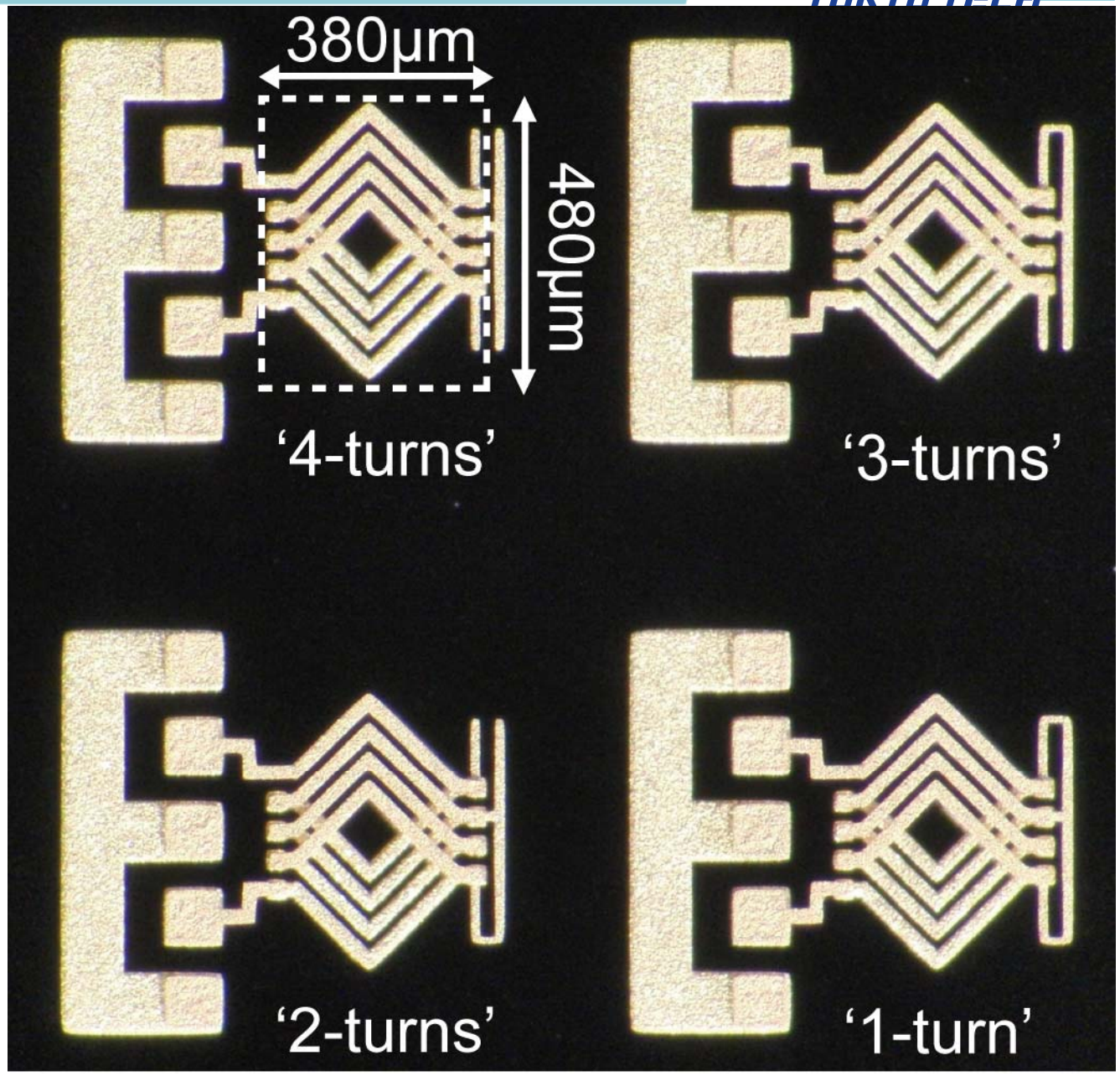
Fabricated test inductors

MEMS process

- Metal（Au）
- Two metal layers
- Substrate:1kΩ・cm

2-bit control

Four test inductors were fabricated



Measurement results of inductance

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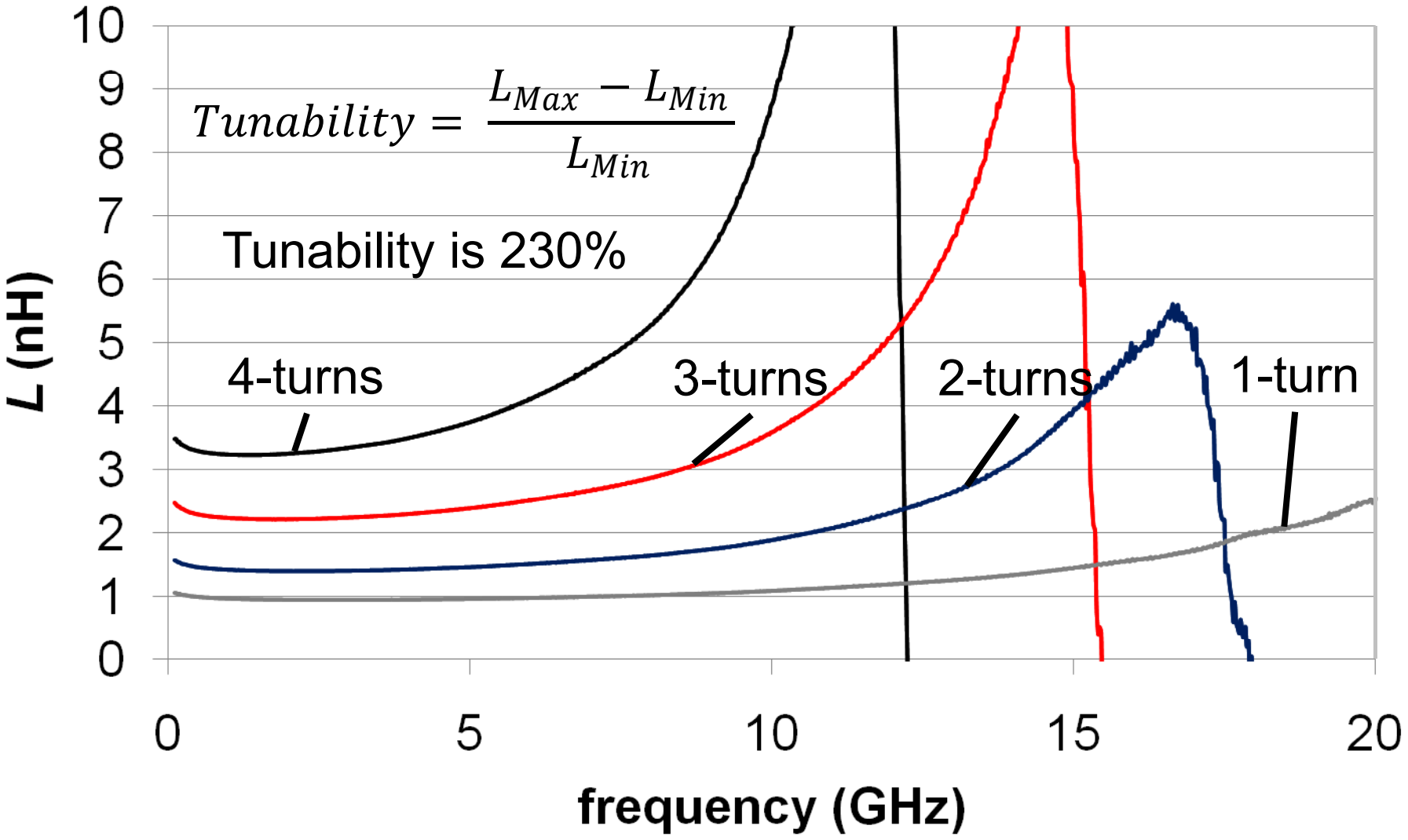

Measurement results of Q-factor

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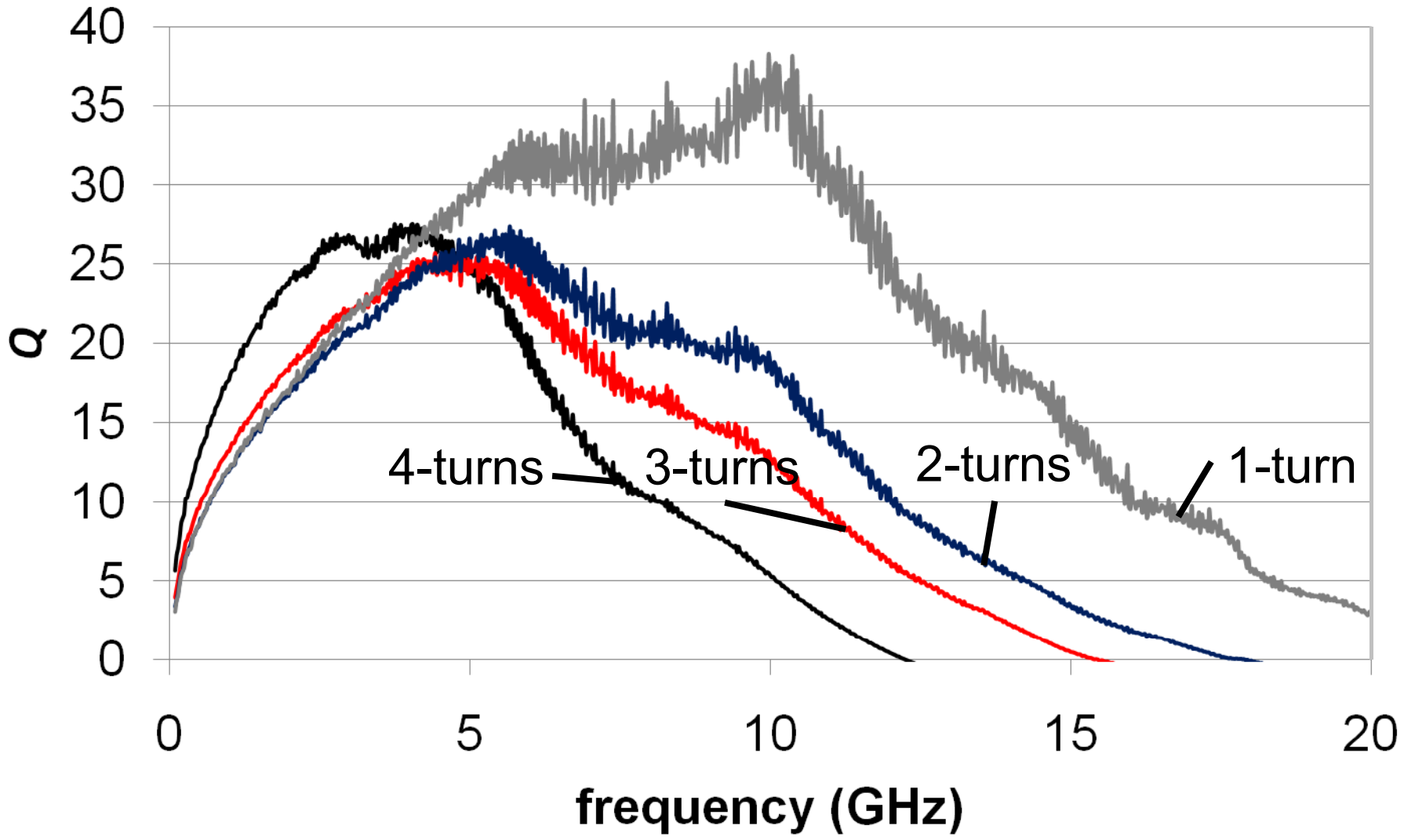
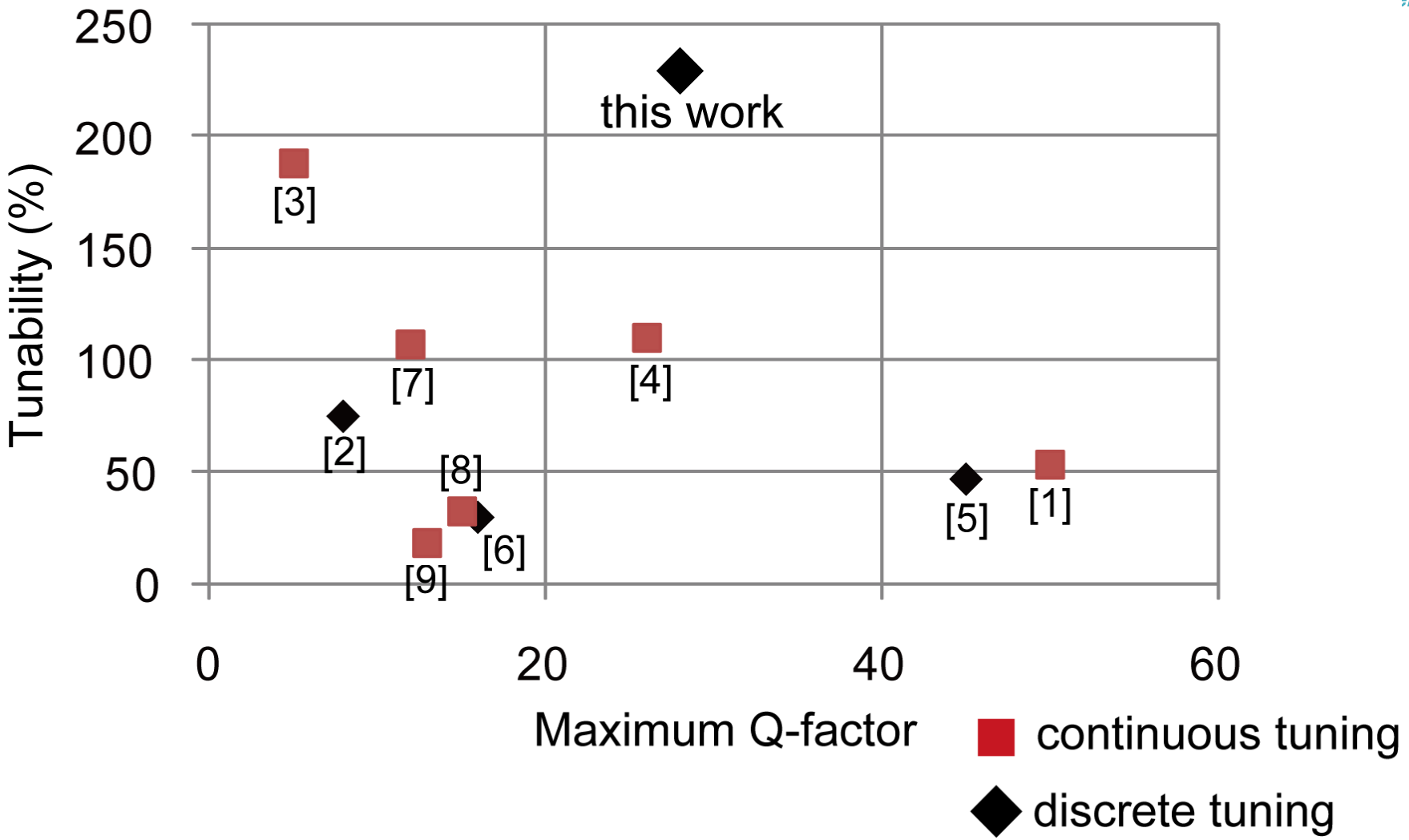


Comparison with other works



[1]: K. Okada, TED, 2006.
[2]: D. H. Choi, Transducers, 2009.
[3]: P. Park, LED, 2004.
[4]: J. Kim, TMTT, 2009.
[5]: M. Rais-Zadeh, JMEMS, 2008.
[6]: A. Shirane, JJAP, 2011.
[7]: I. E. Gmati, mnl, 2010.
[8]: S. Chang, LED, 2006.
[9]: V. M. Lubecke, TMTT, 2001.

Outline

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1. Introduction
2. Our RF CMOS development
   - Why do we expect heterogeneous integration on CMOS ?
3. Our approach to heterogeneous integration: Novel wafer shuttle technique.
4. Summary

How to fabricate functionalities on CMOS

- Issues
  - Do we prepare process equipment?
  - If we have process ability, can we fabricate the functionalities on CMOS **chip** ? Chip sizes are several mm^2.
  - How do we collaborate ? (from the viewpoint of circuit design researcher)

Pre-CMOS and Intermediate- CMOS

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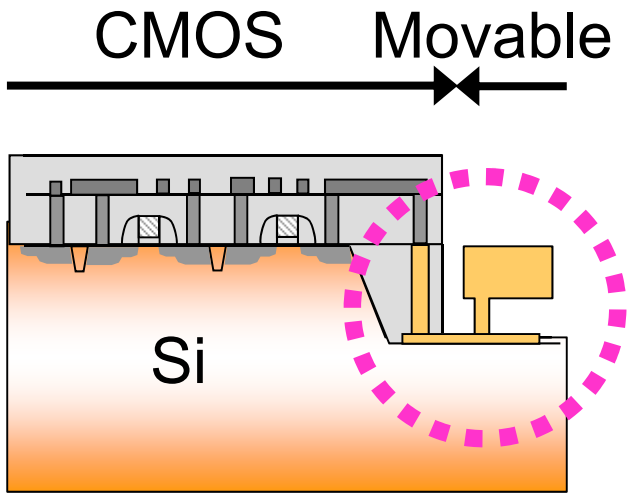
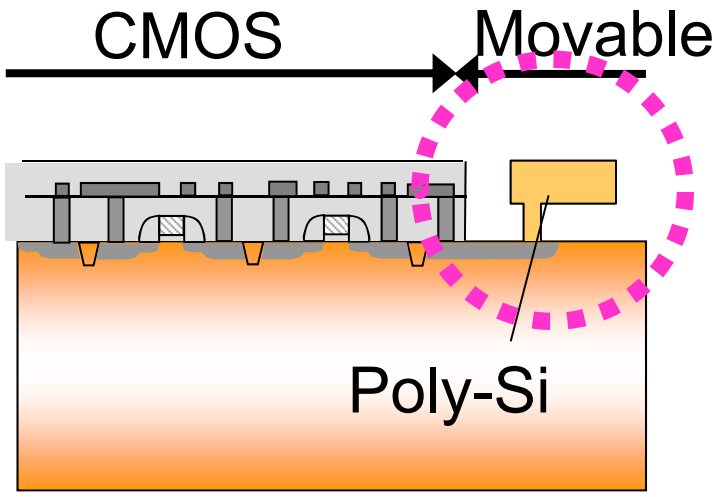
	Pre- CMOS (MEMS first)	Intermediate- CMOS
Structure		
Requirements	・Sealing/Packaging ・Low Voltage ・MOS Reliability ・Sacrificial Film Etching （SiO_2 or SiGe etc.）	・LSI Multilevel Interconnection ・Large Chip Size

Post- CMOS (CMOS-first and MEMS last)

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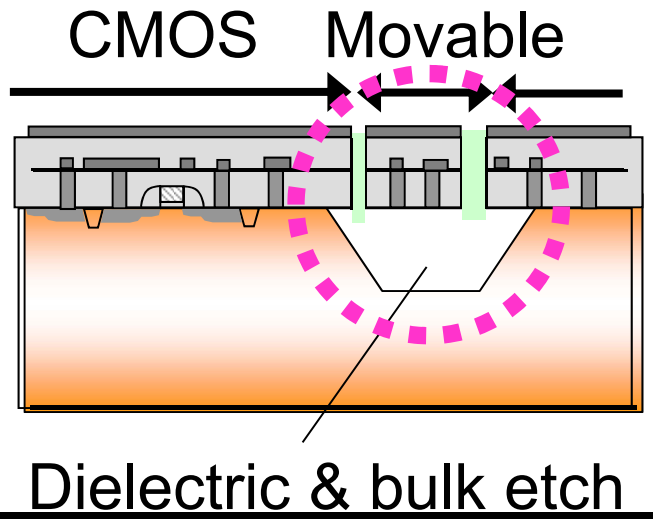
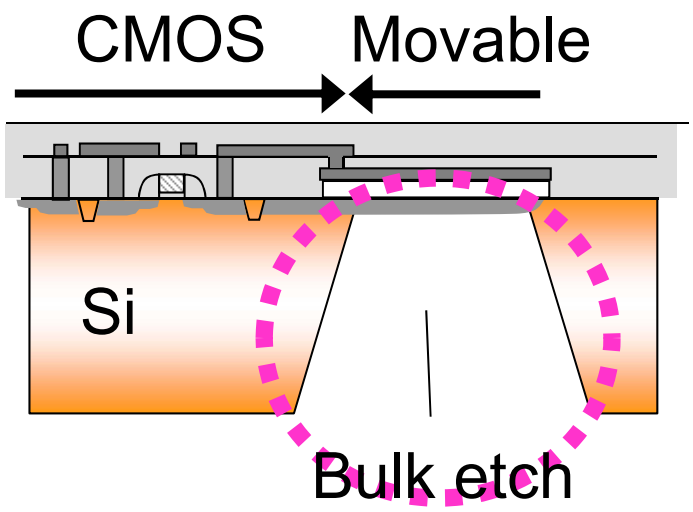
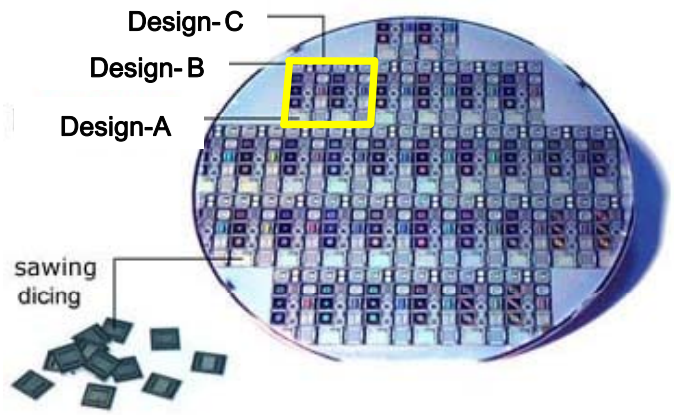
	Etching from Surface	Etching from Back Side
Structure		
Requirements	・Sealing/Packaging ・Low Voltage ・MOS Reliability	・Plasma Damage ・Large Chip Size

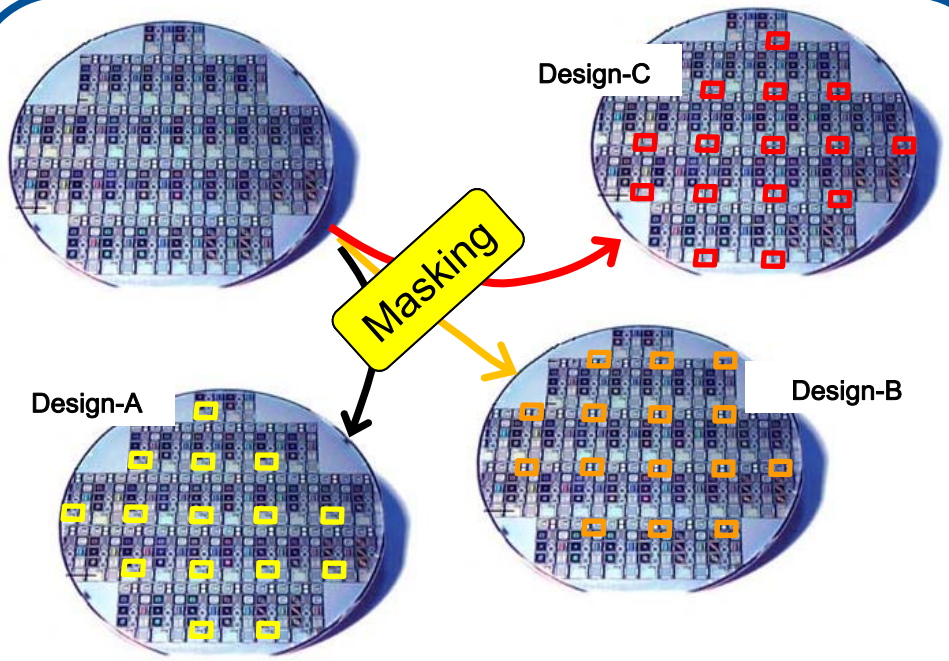
Toward open collaboration

Novel wafer shuttle service for heterogeneous integration



- Designers receive their own circuit as chips.
- Another functions such as sensor, MEMS, photonics etc. cannot be fabricated on the chip.
- So far, CMOS processed wafer cannot be provided because another designer's area cannot be masked.

Conventional shuttle service



- With novel masking technique, wafers can be provided to each designer. In wafer-A, another designer's area are masked.
- Sensor, MEMS, and photonics can be fabricated or implemented on CMOS wafers!

The novel wafer shuttle has been developed by Tokyo Tech/NTT-AT collaboration.

Post CMOS

- MEMS(functionalities)-first is suitable for mass-production type device such as acceleration sensor, pressure sensor, DMD, etc.　cf. DRAM, Flash, MPU
- Post process can open the door to various field researchers: circuit, process, bio engineers.
- New wafer shuttle technology

Detail of wafer shuttle

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- 0.35μm standard CMOS with 20-V MOSFET, 6 inch wafer
- Area designed by another designer is completely masking by the blind process.
- Design and process integration consulting is available thru Tokyo Tech. Standard MEMS is also available.
- PDK is distributed thru VDEC, Univ. Tokyo

CMOS/MEMS standard process

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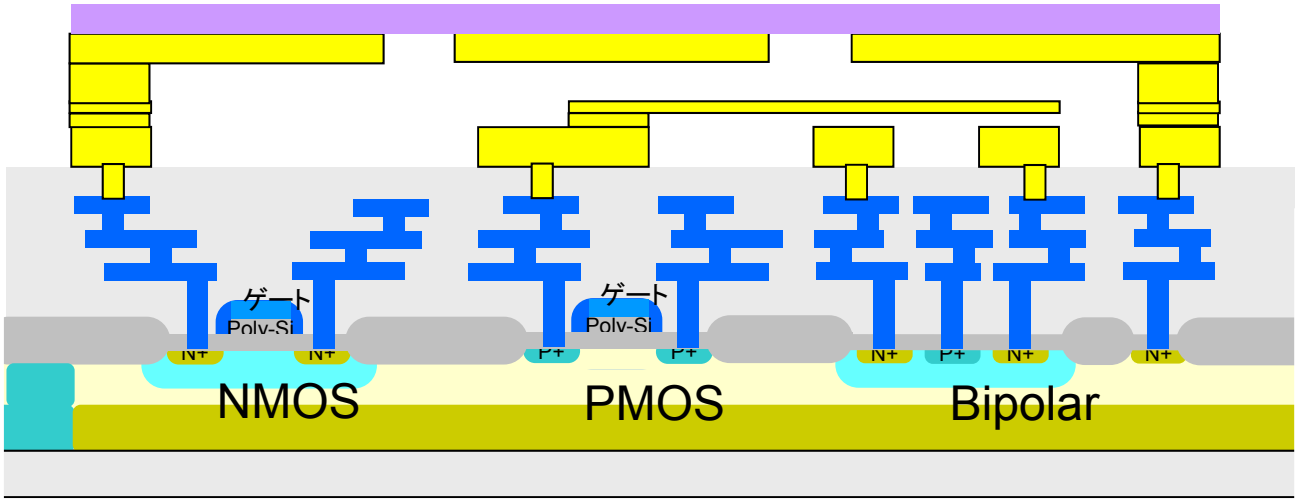
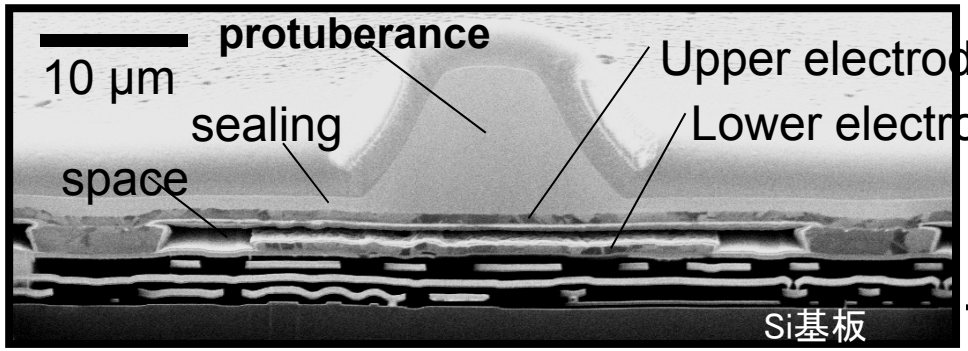
●CMOS-MEMS



MEMS

BiCMOS

●Example of CMOS-MEMS



MEMS

CMOSLSI

Integrated finger print sensor.

Photo: Courtesy of NTT Micro integration Lab.

First wafer shuttle

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- Contributors
  - More than 5 universities
  - More than 3 research group in Tokyo Tech.
- Fields
  - Photonics
  - MEMS
  - RF MEMS
  - Sensors (bio, Hall effect)
- Tape out in Sept, 2011. Wafer will be delivered in Dec. 2011
- Circuit designer provided IPs.

Summary

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- RF CMOS developments:
  - Scalable RF CMOS using miniaturized CMOS
  - Use of functionalities such as RF MEMS inductor
- Wafer shuttle technology
  - First wafer will be delivered in Dec. 2011.
  - Fundamental circuit IPs will be handle by ICE cube center, Tokyo Tech. These IPs will helpful for collaboration of different field researchers.